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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,425	04/10/2006	Sebastien Prouet	FR 030121	3751

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EXAMINER	
POOS, JOHN W	

ART UNIT	PAPER NUMBER
4125	

NOTIFICATION DATE	DELIVERY MODE
12/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/575,425	PROUET ET AL.	
	Examiner	Art Unit	
	JOHN W. POOS	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Differential Input and Output Transconductance Circuit.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Main et al. (US 5,497,123).

In regard to Claim 1:

A transconductance circuit (Figure 3) intended to convert a differential input voltage, supplied as two signals on two inputs, into a differential output current, (Column 5: lines 38-39) characterized in that, where each of the two signals of said differential input voltage is supplied to each input through a follower transistor (Figure 3: 46, 47, 49, 56) connected to said input by its emitter and receives said signal on a control electrode, each of the two inputs of the transconductance is connected to a respective current source that is dynamically controlled by the other input of the transconductance, said current source being such that the current supplied to each input by said current source eliminates current variations caused by voltage variations of the input voltage signal.

In regard to Claim 2 (as taught in Figure 3):

A transconductance circuit as claimed in claim 1, wherein the transconductance circuit comprises two sides, (42 and 43) each side comprising an input (46, 47), an output (44, 45), at least a first transistor (49) having a control electrode coupled for receiving a bias voltage (48), a first electrode connected to said output and a second electrode connected to said input (46 connected to 49 through 51), a second transistor (53) having a first electrode and a control electrode coupled in common to said input (48 connected to 53 through 52), and a second electrode connected to a power supply terminal (53 connected to ground).

In regard to Claim 3:

A transconductance circuit as claimed in claim 2, wherein said first and second transistors are of the same size. (Column 6: lines 6-7)

In regard to Claim 4:

A transconductance circuit as claimed in claim 2, wherein each side further includes a third transistor (Figure 3: 54, 61) of the same size as said second transistor (Column 6: lines 6-7), said third transistor has a control electrode coupled to said first transistor and control electrodes of said second transistor, a first electrode connected to the output of the other side and a second electrode connected to said power supply terminal.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Main et al. (US 5,497,123), in view of Sasaki (US 5,578,943).

In regard to Claim 7:

Main (123) teaches all of the claim limitations as discussed with regard to claim 1 above, except for a chip intended to be implemented in a transceiver including at least a transconductance as claimed in one of the claim 1.

Sasaki (943) teaches a transceiver (Figure 1: transmitter IC (10) and receiver IC (14)) where the signal transmitter comprises a voltage to current converter (Column 1: lines 60-64).

Therefore it would have been obvious to one skilled in the art at the time of the invention to implement a transceiver with a transconductance voltage to current converter in order to provide a current for transmission (Column 1: 60-67)

In regard to Claim 8:

Main (123) teaches all of the claim limitations as discussed with regard to claim 1 above, except for a transceiver of radio-frequency signals including at least one chip as claimed in claim 7.

Sasaki (943) teaches a transceiver (Figure 1: transmitter IC (10) and receiver IC (14)) where the signal transmitter comprises a voltage to current converter (Column 1: lines 60-64).

Therefore it would have been obvious to one skilled in the art at the time of the invention to implement a transceiver with a transconductance voltage to current converter in order to provide a current for transmission (Column 1: 60-67)

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Main et al. (US 5,497,123), in view of Seevinck et al. (US 4,682,098).

In regard to Claim 5:

Main (123) teaches all of the claim limitations as discussed with regard to claim 1 above, except for a transconductance circuit as claimed in one of the claim 2, wherein said current source includes a current mirror mirroring the current passing through said second transistor with a gain of two.

Seevinck (098) teaches a common current source passing $I_2 = 2I_x$ through the emitters of transistors T3 and T4 (Column 3: lines 5-7).

Therefore it would have been obvious to one skilled in the art at the time of the invention to mirror a current with a gain of two through the second transistor in order to supply an output current which is proportional to the signal current (Column 1: lines 21-22).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Main et al. (US 5,497,123) and Seevinck et al. (US 4,682,098), in view of Hughes (US 4,973,857).

In regard to Claim 6:

Main (123) and Seevinck (098) teach all of the claim limitations as discussed with respect to claims 1 and 5 above, except for wherein said current mirror includes a mirror transistor of twice the size of said second transistor.

Hughes (857) teaches the transistor may be bipolar or MOS type (Column 1: liens 22-24) and that the geometry of the channels of MOS transistors can be scaled conveniently to give the desired ratios between the currents in various paths (Column 2: lines 43-45).

Therefore it would have been obvious to one skilled in the art at the time of the invention to used different sized transistors in order to gain the desired ratios between the currents in various paths (Column 2: lines 43-45).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Zarabadi et al. (US 5,151,625) and Stochino (US 6,219,261) both respectively teach differential voltage to current converters.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571) 270-5077. The examiner can normally be reached on M-F (alternating Fridays off), E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. W. P./
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125